MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية					
Module Title	**Logic Design**			**Module Delivery**	
Module Type	**C**			☒ **Theory** ☐ **Lecture** ☒ **Lab** ☒ **Tutorial** ☐ **Practical** ☐ **Seminar**	
Module Code	**AI1204**				
ECTS Credits	**6**				
SWL (hr/sem)	**150**				
Module Level	1		**Semester of Delivery**	2	
Administering Department	AI		**College**	CSIT	
Module Leader	Muhannad Kamel		**e-mail**	muhannad.k@uokerbala.edu.iq	
Module Leader's Acad. Title	Assist Professor		**Module Leader's Qualification**	Ph.D.	
Module Tutor	Muhannad Kamel		**e-mail**	muhannad.k@uokerbala.edu.iq	
Peer Reviewer Name	Ali Mahmoud Ali		**e-mail**	ali.mahmoud@uowa.edu.iq	
Scientific Committee Approval Date	01/03/2026		**Version Number**	1.0	

Relation with other Modules العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	None	**Semester**	
Co-requisites module	None	**Semester**	

Department Head Approval

Dean of the College Approval

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Objectives أهداف المادة الدراسية	1- The student should understand number systems and codes and conversion between them. 2- The student should understand the Boolean expression and how to apply it. 3- The student should recognize among different logic gates and how to use them. 4- The student should understand how to design a logic circuit. 5- The student should understand using K-map for simplification.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	Upon completion of this module, learners will be able to: 1. **Numeric Foundations:** Perform conversions between Binary, Octal, Decimal, and Hexadecimal systems and execute base-specific arithmetic. 2. **Boolean Synthesis:** Apply Boolean algebra theorems and De Morgan's laws to simplify complex logical expressions. 3. **Gate Analysis:** Design and analyze circuits using standard logic gates (AND, OR, NOT) and universal gates (NAND, NOR). 4. **Truth Table Mapping:** Derive standardized Boolean expressions (SOP and POS) from truth tables to define system behavior. 5. **Optimization (K-Maps):** Utilize 2, 3, and 4-variable Karnaugh Maps to minimize gate counts and optimize circuit efficiency. 6. **Algorithmic Minimization:** Apply the Quine-McCluskey method for systematic simplification of logic functions with many variables. 7. **Arithmetic Circuits:** Design fundamental combinational components including Half-Adders, Full-Adders, and Subtractors. 8. **Data Routing:** Implement and configure Decoders, Encoders, Multiplexers (MUX), and De-multiplexers (DEMUX) for signal control. 9. **Sequential Logic:** Differentiate between combinational and sequential logic by understanding the role of memory and feedback in Latches. 10. **Memory Architecture:** Explain the operation of RAM, ROM, and Programmable Logic Devices (PLDs) in digital systems. 11. **System Integration:** Synthesize all concepts to design a functional "Applied Logic" project that solves a specific hardware control problem.
Indicative Contents المحتويات الإرشادية	Introduction to Digital Logic Combinational Logic Design Arithmetic circuits Sequential Logic Design Circuit Testing and Verification
Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	Conceptual Understanding Problem-Solving Approach Hands-on Laboratory Experience Design Projects Simulation and Modeling Problem-Based Learning

Student Workload (SWL) الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا			
Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	93	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	6
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	57	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	4
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	**150**		

Module Evaluation تقييم المادة الدراسية					
		Time/Number	**Weight (Marks)**	**Week Due**	**Relevant Learning Outcome**
Formative assessment	**Quizzes**	5	10% (10)	5 and 10	LO #1, #2 and #10, #11
	Assignments	2	10% (10)	2 and 12	LO #3, #4 and #6, #7
	Projects / Lab.	1	10% (10)	Continuous	All
	Report	1	10% (10)	13	LO #5, #8 and #10
Summative assessment	**Midterm Exam**	2hr	10% (10)	7	LO #1 - #7
	Final Exam	3hr	50% (50)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus) المنهاج الاسبوعي النظري	
	Material Covered
Week 1	Introduction: Digital System
Week 2	Number Systems: Octal and Hexadecimal Numbers
Week 3	Number base conversion
Week 4	● Theories of Boolean Algebra ● Digital Logic gates
Week 5	Boolean Expression and Truth table
Week 6	● Sum of Product Simplification ● Product Of Sum Simplification
Week 7	● Exclusive OR ● NAND gates ● NOR gates
Week 8	Midterm
Week 9	● Two- and Three-Variables Karnaugh Maps. ● Four Variables Karnaugh Maps.

Week 10	Quine-McCluskey method
Week 11	Combinational Logic: Adder, Subtractor Comparators, Decoders and Encoders
Week 12	Multiplexers (Data Selectors). and DE multiplexers
Week 13	Sequential Logic and Latches
Week 14	Applied Logic
Week 15	Memory and Programmable logic

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر	
	Material Covered
Week 1	Codes and conversion among them
Week 2	Codes and conversion among them1
Week 3	Boolean expression
Week 4	Logic gates
Week 5	Circuit Design
Week 6	Second month exam
Week 7	NAND gates & NOR gates
Week 8	Sum of product form
Week 9	Product Of sum form
Week 10	K-map

Learning and Teaching Resources مصادر التعلم والتدريس		
	Text	**Available in the Library?**
Required Texts	An Introduction to Logic Technology by Luois Nashlsky	Yes
Recommended Texts	Fundamentals of logic design by J. Roth	No
Websites	http://www.sasurieengg.com/e-course-material/I-year-E-course-material-II-sem/٧.CS٦٢٠١٪٢٠-DPSD.pdf https://www.scribd.com/doc/٢١٩٥٨٧٥١٩/Digital-Principles-and-System-Dsign https://www.vidyarthiplus.com/vp/thread-١٧٧٨٢.html#.WFrbbFN٩٦po	

Grading Scheme مخطط الدرجات				
Group	**Grade**	التقدير	**Marks %**	**Definition**
Success Group (50 - 100)	**A -** Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX –** Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.