



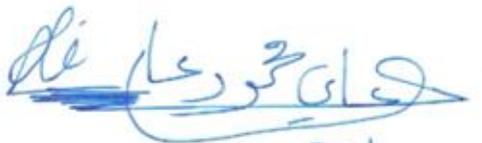
# MODULE DESCRIPTION FORM



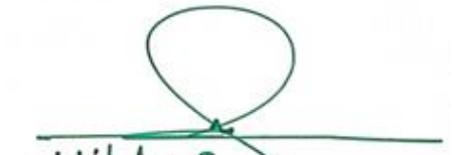
## نموذج وصف المادة الدراسية

Module Information			
معلومات المادة الدراسية			
Module Title	Logic Design		Module Delivery
Module Type	C		<input checked="" type="checkbox"/> Theory <input type="checkbox"/> Lecture <input checked="" type="checkbox"/> Lab <input checked="" type="checkbox"/> Tutorial <input type="checkbox"/> Practical <input type="checkbox"/> Seminar
Module Code	AI1204		
ECTS Credits	6		
SWL (hr/sem)	150		
Module Level	1	Semester of Delivery	
Administering Department	AI	College	CSIT
Module Leader	Muhannad Kamel	e-mail	<a href="mailto:muhannad.k@uokerbala.edu.iq">muhannad.k@uokerbala.edu.iq</a>
Module Leader's Acad. Title	Assist Professor	Module Leader's Qualification	Ph.D.
Module Tutor	Muhannad Kamel	e-mail	<a href="mailto:muhannad.k@uokerbala.edu.iq">muhannad.k@uokerbala.edu.iq</a>
Peer Reviewer Name	Ali Mahmoud Ali	e-mail	<a href="mailto:ali.mahmoud@uowa.edu.iq">ali.mahmoud@uowa.edu.iq</a>
Scientific Committee Approval Date	01/03/2026	Version Number	1.0

Relation with other Modules			
العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	None	Semester	
Co-requisites module	None	Semester	

  
م.م. علي محمود علي  
مقر قسم الذكاء الاصطناعي  
٢٠٢٥ - ٢٠٢٦



  
م.م. محمد علي لفايتي  
العميد  
٢٠٢٥ - ٢٠٢٦

Department Head Approval

Dean of the College Approval

<b>Module Aims, Learning Outcomes and Indicative Contents</b> أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
<b>Module Objectives</b> أهداف المادة الدراسية	1- The student should understand number systems and codes and conversion between them. 2- The student should understand the Boolean expression and how to apply it. 3- The student should recognize among different logic gates and how to use them. 4- The student should understand how to design a logic circuit. 5- The student should understand using K-map for simplification.
<b>Module Learning Outcomes</b> مخرجات التعلم للمادة الدراسية	Upon completion of this module, learners will be able to: <ol style="list-style-type: none"> <li>1. <b>Numeric Foundations:</b> Perform conversions between Binary, Octal, Decimal, and Hexadecimal systems and execute base-specific arithmetic.</li> <li>2. <b>Boolean Synthesis:</b> Apply Boolean algebra theorems and De Morgan's laws to simplify complex logical expressions.</li> <li>3. <b>Gate Analysis:</b> Design and analyze circuits using standard logic gates (AND, OR, NOT) and universal gates (NAND, NOR).</li> <li>4. <b>Truth Table Mapping:</b> Derive standardized Boolean expressions (SOP and POS) from truth tables to define system behavior.</li> <li>5. <b>Optimization (K-Maps):</b> Utilize 2, 3, and 4-variable Karnaugh Maps to minimize gate counts and optimize circuit efficiency.</li> <li>6. <b>Algorithmic Minimization:</b> Apply the Quine-McCluskey method for systematic simplification of logic functions with many variables.</li> <li>7. <b>Arithmetic Circuits:</b> Design fundamental combinational components including Half-Adders, Full-Adders, and Subtractors.</li> <li>8. <b>Data Routing:</b> Implement and configure Decoders, Encoders, Multiplexers (MUX), and De-multiplexers (DEMUX) for signal control.</li> <li>9. <b>Sequential Logic:</b> Differentiate between combinational and sequential logic by understanding the role of memory and feedback in Latches.</li> <li>10. <b>Memory Architecture:</b> Explain the operation of RAM, ROM, and Programmable Logic Devices (PLDs) in digital systems.</li> <li>11. <b>System Integration:</b> Synthesize all concepts to design a functional "Applied Logic" project that solves a specific hardware control problem.</li> </ol>
<b>Indicative Contents</b> المحتويات الإرشادية	Introduction to Digital Logic Combinational Logic Design Arithmetic circuits Sequential Logic Design Circuit Testing and Verification
<b>Learning and Teaching Strategies</b> استراتيجيات التعلم والتعليم	
<b>Strategies</b>	Conceptual Understanding Problem-Solving Approach Hands-on Laboratory Experience Design Projects Simulation and Modeling Problem-Based Learning

<b>Student Workload (SWL)</b> الحمل الدراسي للطلاب محسوب لـ ١٥ اسبوعا			
<b>Structured SWL (h/sem)</b> الحمل الدراسي المنتظم للطلاب خلال الفصل	93	<b>Structured SWL (h/w)</b> الحمل الدراسي المنتظم للطلاب أسبوعيا	6
<b>Unstructured SWL (h/sem)</b> الحمل الدراسي غير المنتظم للطلاب خلال الفصل	57	<b>Unstructured SWL (h/w)</b> الحمل الدراسي غير المنتظم للطلاب أسبوعيا	4
<b>Total SWL (h/sem)</b> الحمل الدراسي الكلي للطلاب خلال الفصل	<b>150</b>		

<b>Module Evaluation</b> تقييم المادة الدراسية					
		Time/Number	Weight (Marks)	Week Due	Relevant Learning Outcome
<b>Formative assessment</b>	<b>Quizzes</b>	5	10% (10)	5 and 10	LO #1, #2 and #10, #11
	<b>Assignments</b>	2	10% (10)	2 and 12	LO #3, #4 and #6, #7
	<b>Projects / Lab.</b>	1	10% (10)	Continuous	All
	<b>Report</b>	1	10% (10)	13	LO #5, #8 and #10
<b>Summative assessment</b>	<b>Midterm Exam</b>	2hr	10% (10)	7	LO #1 - #7
	<b>Final Exam</b>	3hr	50% (50)	16	All
<b>Total assessment</b>			100% (100 Marks)		

<b>Delivery Plan (Weekly Syllabus)</b> المنهاج الاسبوعي النظري	
	Material Covered
<b>Week 1</b>	Introduction: Digital System
<b>Week 2</b>	Number Systems: Octal and Hexadecimal Numbers
<b>Week 3</b>	Number base conversion
<b>Week 4</b>	<ul style="list-style-type: none"> <li>● Theories of Boolean Algebra</li> <li>● Digital Logic gates</li> </ul>
<b>Week 5</b>	Boolean Expression and Truth table
<b>Week 6</b>	<ul style="list-style-type: none"> <li>● Sum of Product Simplification</li> <li>● Product Of Sum Simplification</li> </ul>
<b>Week 7</b>	<ul style="list-style-type: none"> <li>● Exclusive OR</li> <li>● NAND gates</li> <li>● NOR gates</li> </ul>
<b>Week 8</b>	Midterm
<b>Week 9</b>	<ul style="list-style-type: none"> <li>● Two- and Three-Variables Karnaugh Maps.</li> <li>● Four Variables Karnaugh Maps.</li> </ul>

<b>Week 10</b>	Quine-McCluskey method
<b>Week 11</b>	Combinational Logic: Adder, Subtractor Comparators, Decoders and Encoders
<b>Week 12</b>	Multiplexers (Data Selectors). and DE multiplexers
<b>Week 13</b>	Sequential Logic and Latches
<b>Week 14</b>	Applied Logic
<b>Week 15</b>	Memory and Programmable logic

### Delivery Plan (Weekly Lab. Syllabus)

المنهاج الاسبوعي للمختبر

	Material Covered
<b>Week 1</b>	Codes and conversion among them
<b>Week 2</b>	Codes and conversion among them1
<b>Week 3</b>	Boolean expression
<b>Week 4</b>	Logic gates
<b>Week 5</b>	Circuit Design
<b>Week 6</b>	Second month exam
<b>Week 7</b>	NAND gates & NOR gates
<b>Week 8</b>	Sum of product form
<b>Week 9</b>	Product Of sum form
<b>Week 10</b>	K-map

### Learning and Teaching Resources

مصادر التعلم والتدريس

	Text	Available in the Library?
<b>Required Texts</b>	An Introduction to Logic Technology by Luois Nashlsky	Yes
<b>Recommended Texts</b>	Fundamentals of logic design by J. Roth	No
<b>Websites</b>	<a href="http://www.sasurieengg.com/e-course-material/l-year-E-course-material-II-sem/٧.CS٦٢٠١٪٢٠-DPSD.pdf">http://www.sasurieengg.com/e-course-material/l-year-E-course-material-II-sem/٧.CS٦٢٠١٪٢٠-DPSD.pdf</a> <a href="https://www.scribd.com/doc/٢١٩٥٨٧٥١٩/Digital-Principles-and-System-Dsign">https://www.scribd.com/doc/٢١٩٥٨٧٥١٩/Digital-Principles-and-System-Dsign</a> <a href="https://www.vidyarthiplus.com/vp/thread-١٧٧٨٢.html#.WFrbBFN٦٦po">https://www.vidyarthiplus.com/vp/thread-١٧٧٨٢.html#.WFrbBFN٦٦po</a>	

## Grading Scheme

### مخطط الدرجات

Group	Grade	التقدير	Marks %	Definition
<b>Success Group (50 - 100)</b>	<b>A</b> - Excellent	امتياز	90 - 100	Outstanding Performance
	<b>B</b> - Very Good	جيد جدا	80 - 89	Above average with some errors
	<b>C</b> - Good	جيد	70 - 79	Sound work with notable errors
	<b>D</b> - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	<b>E</b> - Sufficient	مقبول	50 - 59	Work meets minimum criteria
<b>Fail Group (0 – 49)</b>	<b>FX</b> – Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	<b>F</b> – Fail	راسب	(0-44)	Considerable amount of work required

**Note:** Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.